74HC4017; 74HCT4017

Johnson decade counter with 10 decoded outputs

Product data sheet

1. General description

The 74HC4017; 74HCT4017 is a high-speed Si-gate CMOS device and is pin compatible with the HEF4017.

The 74HC4017; 74HCT4017 is a 5-stage Johnson decade counter with 10 decoded active HIGH outputs (Q0 to Q9), an active LOW output from the most significant flip-flop ($\overline{Q}$5-9), active HIGH and active LOW clock inputs (CP0 and $\overline{CP}$1) and an overriding asynchronous master reset input (MR).

The counter is advanced by either a LOW-to-HIGH transition at CP0 while $\overline{CP}$1 is LOW or a HIGH-to-LOW transition at $\overline{CP}$1 while CP0 is HIGH (see Table 3).

When cascading counters, the $\overline{Q}$5-9 output, which is LOW while the counter is in states 5, 6, 7, 8 and 9, can be used to drive the CP0 input of the next counter.

A HIGH on MR resets the counter to zero (Q0 = $\overline{Q}$5-9 = HIGH; Q1 to Q9 = LOW) independent of the clock inputs (CP0 and $\overline{CP}$1).

Automatic code correction of the counter is provided by an internal circuit: following any illegal code the counter returns to a proper counting mode within 11 clock pulses.

2. Features

- Multiple package options
- Complies with JEDEC standard no. 7 A
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

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3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC4017				
74HC4017N	–40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74HC4017D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC4017DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HC4017PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HC4017BQ	–40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal-enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1
74HCT4017				
74HCT4017N	–40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74HCT4017D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT4017BQ	–40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal-enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

4. Functional diagram

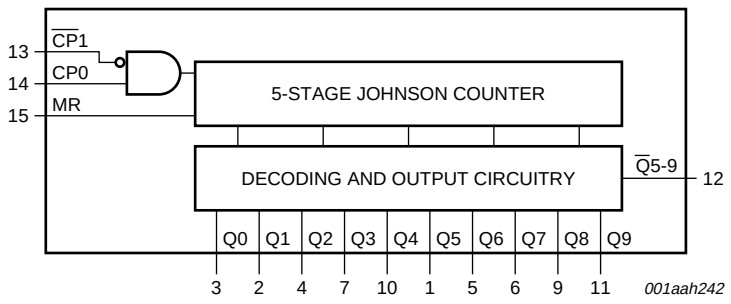

Fig 1. Functional diagram

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6. Functional description

Table 3. Function table[1]

MR	CP0	$\overline{CP1}$	Operation
H	X	X	Q0 = $\overline{Q}$5-9 = HIGH; Q1 to Q9 = LOW
L	H	↓	counter advances
L	↑	L	counter advances
L	L	X	no change
L	X	H	no change
L	H	↑	no change
L	↓	L	no change

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care;
↑ = LOW-to-HIGH transition;
↓ = HIGH-to-LOW transition;

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_O	output current	-0.5 V $< V_O < V_{CC} + 0.5$ V		-	±25	mA
I_{CC}	supply current			-	50	mA
I_{GND}	ground current			–50	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C				
	DIP16 package		[2]	-	750	mW
	SO16 package		[3]	-	500	mW
	(T)SSOP16 package		[4]	-	500	mW
	DHVQFN16 package		[5]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] P_{tot} derates linearly with 12 mW/K above 70 °C.

[3] P_{tot} derates linearly with 8 mW/K above 70 °C.

[4] P_{tot} derates linearly with 5.5 mW/K above 60 °C.

[5] P_{tot} derates linearly with 4.5 mW/K above 60 °C.

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8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
74HC4017						
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	ns/V
		V_{CC} = 4.5 V	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	ns/V
T_{amb}	ambient temperature		–40	-	+125	°C
74HCT4017						
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 4.5 V	-	1.67	139	ns/V
T_{amb}	ambient temperature		–40	-	+125	°C

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC4017										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = –20 µA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = –20 µA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = –20 µA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = –4.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V

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Table 6. Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		I_O = 20 µA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	-	80	-	160	µA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT4017										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V								
		I_O = –20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = –4 mA	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V								
		I_O = 20 µA	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V; I_O = 0 A	-	-	8.0	-	80	-	160	µA
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC}$ – 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V; I_O = 0 A								
		CP0 input	-	25	90	-	113	-	123	µA
		$\overline{CP}$1 input	-	40	144	-	180	-	196	µA
		MR input	-	50	180	-	225	-	245	µA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

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10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; see Figure 11.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC4017										
t_{pd}	propagation delay	CP0 to Qn; CP0 to $\overline{Q}$5-9; [1] see Figure 10								
		V_{CC} = 2.0 V	-	63	230	-	290	-	345	ns
		V_{CC} = 4.5 V	-	23	46	-	58	-	69	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	20	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	18	39	-	49	-	59	ns
		$\overline{CP}$1 to Qn; $\overline{CP}$1 to $\overline{Q}$5-9; see Figure 10								
		V_{CC} = 2.0 V	-	61	250	-	315	-	375	ns
		V_{CC} = 4.5 V	-	22	50	-	63	-	75	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	20	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	18	43	-	54	-	64	ns
t_{PHL}	HIGH to LOW propagation delay	MR to Q[1:9]; see Figure 10								
		V_{CC} = 2.0 V	-	52	230	-	290	-	345	ns
		V_{CC} = 4.5 V	-	19	46	-	58	-	69	ns
		V_{CC} = 6.0 V	-	15	39	-	49	-	59	ns
t_{PLH}	LOW to HIGH propagation delay	MR to $\overline{Q}$5-9, Q0; see Figure 10								
		V_{CC} = 2.0 V	-	55	230	-	290	-	345	ns
		V_{CC} = 4.5 V	-	20	46	-	58	-	69	ns
		V_{CC} = 6.0 V	-	16	39	-	49	-	59	ns
t_t	transition time	see Figure 10 [2]								
		V_{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V	-	6	13	-	16	-	19	ns
t_W	pulse width	CP0 and $\overline{CP}$1 (HIGH or LOW); see Figure 9								
		V_{CC} = 2.0 V	80	17	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	6	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	5	-	17	-	20	-	ns
		MR (HIGH); see Figure 9								
		V_{CC} = 2.0 V	80	19	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	7	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	6	-	17	-	20	-	ns

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Table 7. Dynamic characteristics *…continued*

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; see Figure 11.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{su}	set-up time	$\overline{CP}$1 to CP0; CP0 to $\overline{CP}$1; see Figure 8								
		V_{CC} = 2.0 V	50	–8	-	65	-	75	-	ns
		V_{CC} = 4.5 V	10	–3	-	13	-	15	-	ns
		V_{CC} = 6.0 V	9	–2	-	11	-	13	-	ns
t_h	hold time	$\overline{CP}$1 to CP0; CP0 to $\overline{CP}$1; see Figure 8								
		V_{CC} = 2.0 V	50	17	-	65	-	75	-	ns
		V_{CC} = 4.5 V	10	6	-	13	-	15	-	ns
		V_{CC} = 6.0 V	9	5	-	11	-	13	-	ns
t_{rec}	recovery time	MR to CP0 and MR to $\overline{CP}$1; see Figure 9								
		V_{CC} = 2.0 V	5	–17	-	5	-	5	-	ns
		V_{CC} = 4.5 V	5	–6	-	5	-	5	-	ns
		V_{CC} = 6.0 V	5	–5	-	5	-	5	-	ns
f_{max}	maximum frequency	CP0 or $\overline{CP}$1; see Figure 9								
		V_{CC} = 2.0 V	6.0	23	-	4.8	-	4.0	-	MHz
		V_{CC} = 4.5 V	30	70	-	24	-	20	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF	-	77	-	-	-	-	-	MHz
		V_{CC} = 6.0 V	25	83	-	28	-	24	-	MHz
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}; V_{CC} = 5 V; f_i = 1 MHz [3]	-	35	-	-	-	-	-	pF
74HCT4017										
t_{pd}	propagation delay	CP0 to Qn; CP0 to $\overline{Q}$5-9; see Figure 10 [1]								
		V_{CC} = 4.5 V	-	25	46	-	58	-	69	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	21	-	-	-	-	-	ns
		$\overline{CP}$1 to Qn; $\overline{CP}$1 to $\overline{Q}$5-9; see Figure 10								
		V_{CC} = 4.5 V	-	25	50	-	63	-	75	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	21	-	-	-	-	-	ns
t_{PHL}	HIGH to LOW propagation delay	MR to Q[1:9]; see Figure 10								
		V_{CC} = 4.5 V	-	22	46	-	58	-	69	ns
t_{PLH}	LOW to HIGH propagation delay	MR to $\overline{Q}$5-9, Q0; see Figure 10								
		V_{CC} = 4.5 V	-	20	46	-	58	-	69	ns

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Table 7. Dynamic characteristics *…continued*

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; see Figure 11.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_t	transition time	see Figure 10 [2]								
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
t_W	pulse width	CP0 and $\overline{CP1}$ (HIGH or LOW); see Figure 9								
		V_{CC} = 4.5 V	16	7	-	20	-	24	-	ns
		MR (HIGH); see Figure 9								
		V_{CC} = 4.5 V	16	4	-	20	-	24	-	ns
t_{su}	set-up time	$\overline{CP1}$ to CP0; CP0 to $\overline{CP1}$; see Figure 8								
		V_{CC} = 4.5 V	10	–3	-	13	-	15	-	ns
t_h	hold time	$\overline{CP1}$ to CP0; CP0 to $\overline{CP1}$; see Figure 8								
		V_{CC} = 4.5 V	10	6	-	13	-	15	-	ns
t_{rec}	recovery time	MR to CP0 and MR to $\overline{CP1}$; see Figure 9								
		V_{CC} = 4.5 V	5	–5	-	5	-	5	-	ns
f_{max}	maximum frequency	CP0 or $\overline{CP1}$; see Figure 9								
		V_{CC} = 4.5 V	30	61	-	24	-	20	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF	-	67	-	-	-	-	-	MHz
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC} – 1.5 V; V_{CC} = 5 V; f_i = 1 MHz [3]	-	36	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.

[2] t_t is the same as t_{THL} and t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

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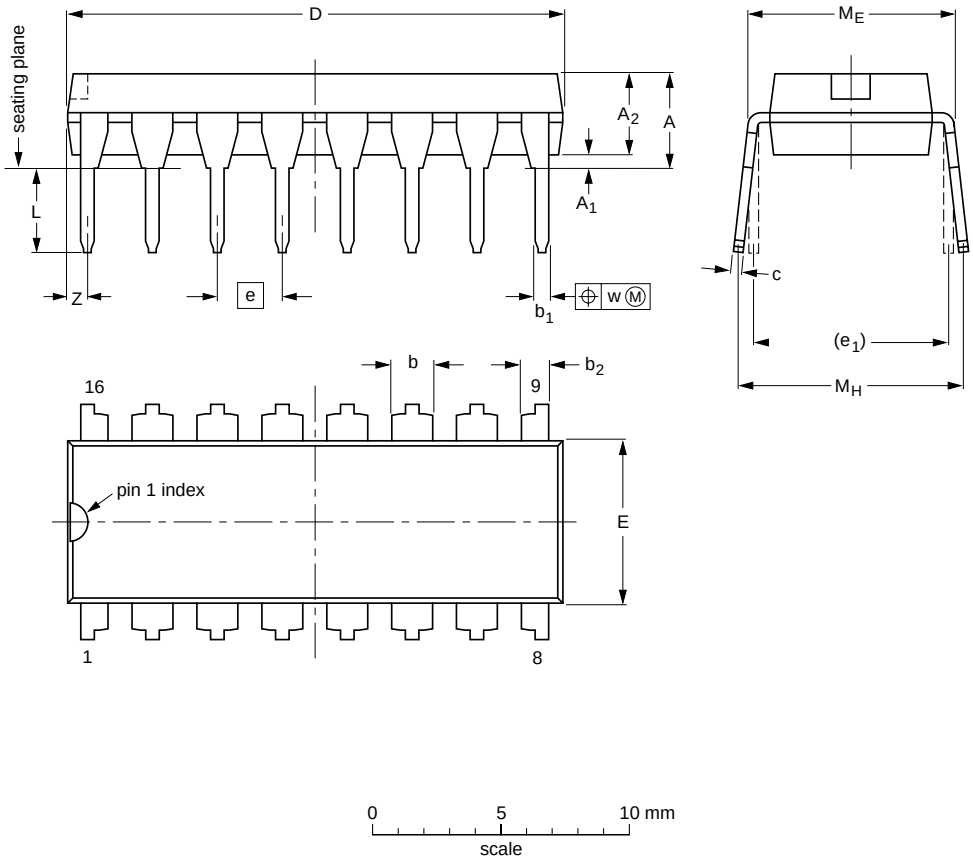
13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	
	IEC	JEDEC	JEITA			
SOT38-4						

Fig 14. Package outline SOT38-4 (DIP16)

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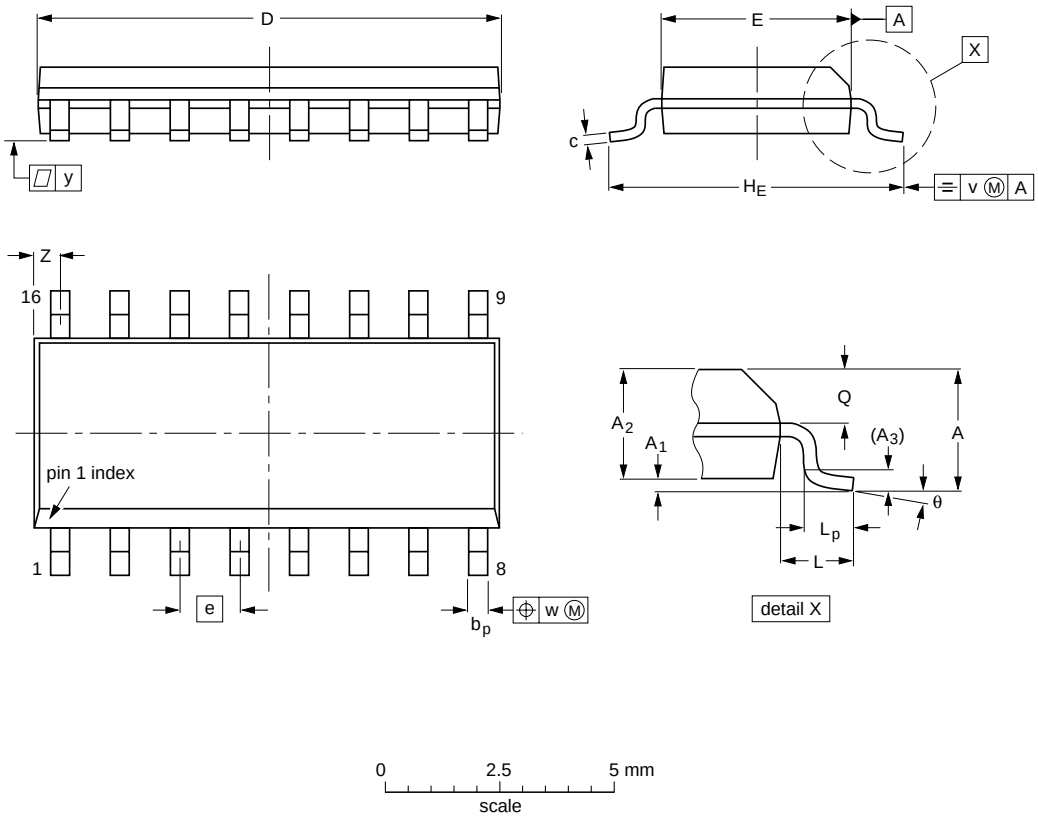
SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				

Fig 15. Package outline SOT109-1 (SO16)

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